Fabricating Capacitive Micromachined Ultrasonic Transducers With Wafer-Bonding Technology

Yongli Huang, A. Sanli Ergun, Edward Hæggström, Mohammed H. Badi, and B. T. Khuri-Yakub

***Abstract*—This paper introduces a new method for fabricating capacitive micromachined ultrasonic transducers (CMUTs) that uses a wafer bonding technique. The transducer membrane and cavity are defined on an SOI (silicon-on-insulator) wafer and on a prime wafer, respectively. Then, using silicon direct bonding in a vacuum environment, the two wafers are bonded together to form a transducer. This new technique, capable of fabricating large CMUTs, offers advantages over the traditionally micromachined CMUTs. First, forming a vacuum-sealed cavity is relatively easy since the wafer bonding is performed in a vacuum chamber. Second, this process enables better control over the gap height, making it possible to fabricate very small gaps (less than 0.1 μm). Third, since the membrane is made of single crystal silicon, it is possible to predict and control the mechanical properties of the membrane to within 5%. Finally, the number of process steps involved in making a CMUT has been reduced from 22 to 15, shortening the device turn-around time. All of these advantages provide repeatable fabrication of CMUTs featuring predictable center frequency, bandwidth, and collapse voltage. Using this new technique, we have fabricated CMUTs that have membrane sizes between 12 μm and 750 μm, and thicknesses between 0.34 μm and 4.5 μm. This paper presents the fabrication process and some experimental results obtained from the wafer-bonded devices. [929]**

***Index Terms*—Capacitive micromachined ultrasonic transducers (CMUT), silicon-on-insulator (SOI) wafer, ultrasonic transducer, wafer bonding.**

I. INTRODUCTION

A CAPACITIVE micromachined ultrasonic transducer (CMUT) is a device where two plate-like electrodes are biased after which an ac signal is applied on top of the dc bias to harmonically move one of the plates. The main parts of a CMUT are the cavity, the membrane and the electrode, Fig. 2 [1].

CMUTs have been considered an attractive alternative to conventional piezoelectric transducers in many areas of application [2]. Micromachined CMUTs provide the following advantages over piezoelectric transducers: CMUTs can be batch produced with a standard IC process to tight parameter specifications, which is difficult with lead zirconium titanate transducers, PZTs [3]. This means that near-electronics can be integrated with the transducer [4]. It is easier to make transducer arrays from CMUTs than from PZTs [3]. Moreover, a CMUT can operate in a wider temperature range than a PZT device [3]. Furthermore, the acoustic impedance match of a CMUT to air is closer than that of PZT transducers, due to the small mechanical impedance of the thin transducer membrane [5].

Active research on CMUTs has been reported in the last decade [6]–[8]. Recently, surface micromachined CMUTs have been successfully fabricated and tested in air and in water [6], [9]. These results demonstrate that CMUTs optimized with respect to such design parameters as device size, membrane radius, thickness, shape, gap height, and region of operation can perform comparably to piezoelectric transducers in terms of bandwidth, frequency range, and dynamic range.

Surface micromachining has met with success as a means to fabricate CMUTs. There are, however, problems associated with this technology in relation to CMUT fabrication. The surface micromachining process introduces limitations on the cavity and membrane size of a CMUT [10].

The traditional fabrication process sets limitations to the fabrication of both low frequency and high frequency devices. Low frequency devices feature large membranes with large residual stresses. Moreover, releasing these membranes is difficult due to large capillary forces causing stiction during the drying process [11]–[13]. With high-frequency devices the process limitation stems from a decrease in relative active area of the devices when the membrane size is reduced.

In the wafer-bonding technique, the membrane and the cavity are defined on separate wafers that are bonded under vacuum conditions. Wafer bonding has previously been employed in the fabrication of low frequency loudspeakers [14] and microphones [15], but not in the fabrication of CMUTs. The wafer-bonding technique can simplify the CMUT fabrication process. The new technique reduces the number of process steps as well as provides solutions for many of the aforementioned problems. The wafer-bonding technique when employed for CMUT production should be able to provide faster processing albeit with higher initial costs in the form of expensive SOI wafers.

In this work, CMUTs designed for sub-MHz operation are, to our knowledge, fabricated by a wafer bonding technique for the first time. The fabricated devices are mechanically and electrically characterized in order to assess their function. The emphasis of this paper is on the fabrication of the devices with the wafer bonding technique.

II. MOTIVATION

There are a several advantages associated with fabrication of CMUTs by wafer-bonding technology:

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A. Vacuum Cavity Formation

Traditionally, the vacuum cavity is formed as follows. First, a sacrificial layer is deposited and patterned into the membrane shape. Next, the membrane that conformably covers the sacrificial layer is deposited. Later, a small hole is etched through the membrane to access the sacrificial layer. The sacrificial layer is removed, and the membrane is released with a wet etch process. The small etch hole is subsequently sealed under vacuum to create a vacuum sealed gap between the membrane and the substrate. These steps introduce fabrication limitations to the traditional process, due to long etch times.

With wafer bonding, it is easier and faster to form a vacuum cavity than it is with the surface micromachining process. The new technique could make the sealing process with its complex via open and refill process obsolete [4].

Wafer bonding also avoids adding unwanted material, such as LTO or Si_3N_4, onto the membrane's inner surface during the via refill process [16]. This should result in higher thickness uniformity across individual membranes and in higher thickness conformity between the membranes in a device.

B. Cavity Size and Shape

There are three advantages in forming the cavity with the wafer bonding technique. First, the cavity shape is independent of the membrane shape. The benefit of this is that one can separately optimize the design parameters (shape, size and height) of the cavity and membrane without any trade-off between them. Second, the aspect ratio of the cavity is no longer limited by the height of the sacrificial layer that can be deposited. Nor is it limited by the slow sacrificial layer etch. Finally, there is no unwanted material deposition onto the faces of the gap which results in a more accurate control over the gap height. A good control of the depth of the cavity makes it possible to fabricate large gaps with high precision. This means a better control over the operating voltage and the electromechanical coupling coefficient of the device [2].

C. Membrane Size and Shape

The largest CMUT membranes currently fabricated with the traditional fabrication process feature a 180-μm-diameter, 3-μm -thick membrane. This is due to both stress release and stiction problems. The high stresses involved with thin film depositions make it difficult and unpractical to deposit arbitrarily thick sacrificial layers, while both the stress and stiction problems make it difficult to release large membranes [11]–[13]. By using the wafer bonding technique one can avoid the wet sacrificial layer etch and its associated problems, and fabricate very large membranes.

Since the CMUT membranes and cavities are fabricated on different wafers before bonding, the wafer bonding technique provides flexibility to design CMUTs with membranes of different size, and shape. This is due to the fact that the membrane is the active layer in the SOI wafer, which can be formed at will, independent of the cavity size and shape. All this translates into fewer limitations on the device design when trying to obtain a desired dynamic response. Moreover, by avoiding the traditional slow releasing process (up to seven days), the turn around time is significantly improved.

D. Membrane Material

In the traditional CMUT fabrication process, the silicon nitride membrane is deposited using low pressure chemical vapor deposition (LPCVD). Ammonia (NH_3) and dichlorosilane $(SiCl_2H_2)$ are brought together into a reactor at 800 °C to deposit the silicon nitride layer on the wafer. The temperature of the reactor and the concentrations of the gases determine the electrical and mechanical properties of the silicon nitride, including its residual stress. Low stress silicon nitride films deposited in this way turn out with 100 MPa of residual stress [17]. Even if the deposition conditions, i.e., temperature, pressure and gas fractions, are adjusted to achieve low internal stress, the resulting membranes are limited in size by the sacrificial release process. Moreover, the mechanical properties of the resulting silicon nitride membrane are less well known and controlled than these of single crystal silicon. When a low residual stress is desired, the process tends to generate amorphous membranes with poorly defined mechanical properties.

In the wafer-bonding process, the membrane is made from single crystal silicon, which has desirable mechanical properties, e.g., few internal defects, low internal mechanical loss, and very low internal stress. This will improve the device reliability, especially important with large devices with thousands of membranes, as well as the performance of the device. Lattice defects act as breakage nuclei while lower internal loss increases the electromechanical coupling efficiency of the device.

By using an SOI wafer to form the membrane, one can achieve a good thickness uniformity (better than 2.5% of the thickness is commercially available), controllability of the stress in the membrane, and process repeatability. This is relevant with respect to commercialization of CMUT fabrication.

E. Fill Factor

Because the vacuum cavity is formed during the wafer bonding process, the complex etch channel structure [4] is no longer needed. The area occupied by these structures can be partially utilized as active transducer area in the wafer-bonded CMUT (73% active area compared to 56%, with 12 μm membrane and 2 μm post width). This effect is more pronounced when fabricating high-frequency devices featuring small membranes each of which requires these channel structures.

Exploring the above presented advantages, CMUTs can be designed and fabricated to meet specifications in different application areas, e.g., sensing in low pressure or high-pressure environment and high-power applications.

III. Fabrication Process

Fabricating CMUTs by the wafer-bonding technique is a four-mask process as shown in Fig. 1. The process starts with a low resistivity, 0.008–0.02 Ω/square, 4-in N-type $\langle 100 \rangle$ silicon wafer that is the future bottom electrode. The first step (Step 1) is to grow silicon dioxide at 1100 °C on the silicon wafer prior to cavity definition. Depending on the required cavity depth of the CMUT, one of two different processes is used to form the cavity before wafer bonding. After the cavity definition, the two processes are identical.

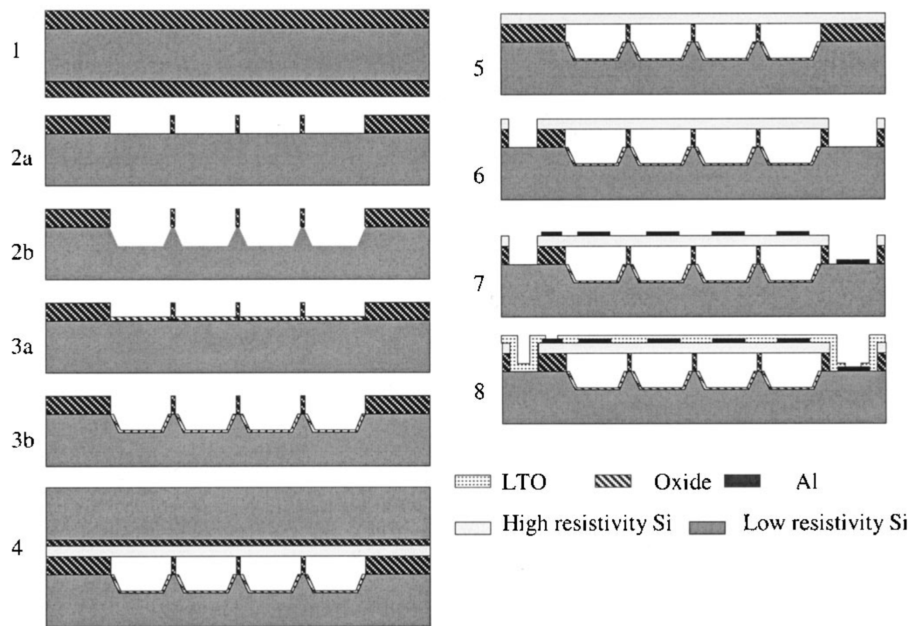

Fig. 1. The steps to fabricate wafer bonded CMUTs: 1. Thermal oxidation. 2a. Thermal oxide etch to define the cavity. 3a. Thermal oxidation for electrical isolation. 2b. Silicon etch to define the deep cavity. 3b. Thermal oxidation for electrical isolation. 4. Silicon wafer fusion bond. 5. Ground/etch back and remove the box. 6. Silicon/oxide etch. 7. Aluminum deposition and patterning. 8. LTO deposition and patterning.

If the required cavity depth is less than 2 μm, the cavity is formed in the oxide layer (Step 2a). The oxide layer is patterned with photolithography (Mask 1) and etched with buffered oxide etch (6:1 BOE) that stops on the silicon surface. Therefore, the cavity depth is determined by the thickness of the oxide layer. After photoresist removal, another thermal oxide layer is grown (1200 Å, Step 3a) as an electrical isolation layer for the CMUT. The wafer is ready for wafer bonding.

If the required cavity depth is more than 2 μm, the cavity is defined by silicon etching (Step 2b). A 1200 Å thermal oxide layer is grown to protect the silicon surface and used as the hard mask for silicon etching in potassium hydroxide (KOH). The KOH etch that is done at 70°C is followed by 6:1 BOE etch to remove the oxide. A 4000 Å thermal oxide layer is grown (Step 3b) at 1100°C as electrical isolation and the wafer is ready for wafer bonding.

The surface finish and cleanliness is of utmost importance for wafer bonding. Therefore, prior to the bonding, the wafer surface is cleaned and activated; first, in Piranha (4:1 Sulfuric Acid: Hydrogen Peroxide) for 20 min, then in 50:1 hydrofluoric acid (HF) for 15 seconds. Finally, the wafer surfaces are treated in RCA1 for 5 min. The wafer bonding is done with a bonder at 10^{-5} mbar vacuum, at a temperature of 150 °C (Step 4). The bonded wafers are then annealed at 1100 °C for two hours to make the bond permanent. After this, the wafers are ground and etched back (using KOH) to the box (oxide layer) of the SOI wafer to form the membrane (Step 5). The box layer is removed with 6:1 BOE. This completes the membrane fabrication. In order to secure thorough bonding everywhere, the thin membranes are allowed to be pushed by the atmospheric pressure toward the posts and a postanneal is performed to improve the bond between the membrane and the thin posts is obtained.

The active silicon layer is subsequently patterned by photolithography (Mask 2) and plasma etching (Step 6). One purpose of the etching is to open a via through the top layers to contact the bottom electrode of the CMUT. Another purpose is to make an isolation trench between devices. After this, 3300 Å aluminum is sputtered by a metal sputter system and patterned (Mask 3) to serve as the top electrode for the CMUT (Step 7). The sputtering is followed by a step where 4000 Å of low temperature oxide (LTO) is deposited as a passivating layer. Then, the LTO layer is patterned (Mask 4) to open pads for wire bonds (Step 8).

IV. Device Design and Fabrication

The design effort is based on exploiting the physics of the CMUT, Fig. 2. The operation of a CMUT relies on the electrostatic force. When a dc voltage is applied between the bottom surface of the cavity and the membrane electrode, the membrane deflects toward the substrate (the hot electrode). The electrostatic force is balanced by a restoring mechanical force due to the increased strain in the membrane. The amount of deflection can be calculated from the bulk modulus of the membrane and the geometry [18].

The membrane can be set into motion by adding a small ac signal on top of the dc bias voltage. The vibrating membrane then couples mechanical energy into the surrounding medium. This energy transfer can be estimated to first order from the real part of the device impedance, since at resonance the only resistive parts in the CMUT model [6] are the internal losses in the membrane and the acoustic radiation. CMUT operation is described in [2], [4], [6]. Another measure of the transduction efficiency of a CMUT is its electromechanical coupling coefficient, ${k_T}^2$. This parameter indicates how efficiently the electrical energy applied to the device is converted into mechanical energy of the membrane [18]. ${k_T}^2$ increases with increasing dc bias voltage [10], and can be obtained from the capacitance versus bias voltage curve [19].

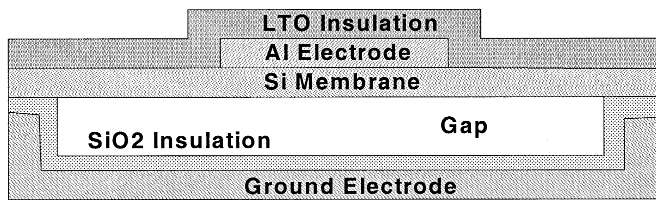

Fig. 2. The cross-sectional schematics of a CMUT.

The maximum bias voltage that can be applied to a CMUT is limited, however. The reason is that a high dc voltage results in a large electrostatic force that stretches the membrane toward the substrate. Close to the substrate, the electrostatic force that is inversely proportional to the separation between the electrodes, increases. The restoring mechanical force is proportional to the membrane deflection for small membrane deflections [20]. Hence, there exists a bias voltage where the mechanical restoring force of the membrane cannot balance the electrostatic force. This voltage is called the collapse voltage of the membrane [20]. When a bias voltage higher than the collapse voltage is applied, the membrane collapses to the substrate and does not vibrate in its fundamental mode. The collapsed membrane can be restored to its noncollapsed state by lowering the bias voltage. At a certain voltage, called snapback voltage, that is clearly lower than the collapse voltage, the membrane snaps back to a noncollapsed state [21], [22].

A CMUT cannot be traditionally operated beyond the collapse voltage. Therefore in order to maximize the ${k_T}^2$ value of the device, the bias voltage has to be close to, but lower than, the collapse voltage [2], [18]. An important aspect of the CMUT design is to keep this voltage low to enable low-voltage operation. Low-voltage operation is advantageous with respect to power consumption, electronic circuitry (switches), and safety.

The mechanical restoring force of the membrane, together with its thickness and mass, determine the dynamic behavior of the membrane and its frequency characteristics [16]. Therefore, CMUT design starts with the design of the geometrical parameters of the membrane. Specifically, the size and the thickness of the membrane are optimized for performance. The cavity beneath the membrane is vacuum sealed. Therefore, the membrane deflects under ambient pressure. The design of the gap has two considerations. The gap should be wide enough so that when the membranes are deflected under ambient pressure, they do not touch the substrate. Furthermore, it should not be too wide as to prevent low voltage operation.

We have calculated the static deflection of the membranes under ambient pressure and their corresponding collapse voltages are calculated and optimized using finite element analysis [23], [24]. Moreover, ANSYS simulations were performed to predict resonance frequency and ${k_T}^2$ of the designed devices, cf. Table II. The stress distribution over the membranes, shown in Fig. 9 was also simulated in order to avoid membrane cracking along the edges of the supporting posts where the tensile stress is highest. Circular and square membranes were simulated since the former features the lowest possible local stress while the latter features the largest possible local stress.

Two fabrication runs were carried out to test the potential of the new technique. The first run aimed at producing, for comparison, devices operating above 1 MHz in air, which could have been produced by the traditional fabrication process as well. The second run aimed at producing low frequency devices that could not have been produced by the traditional fabrication technique.

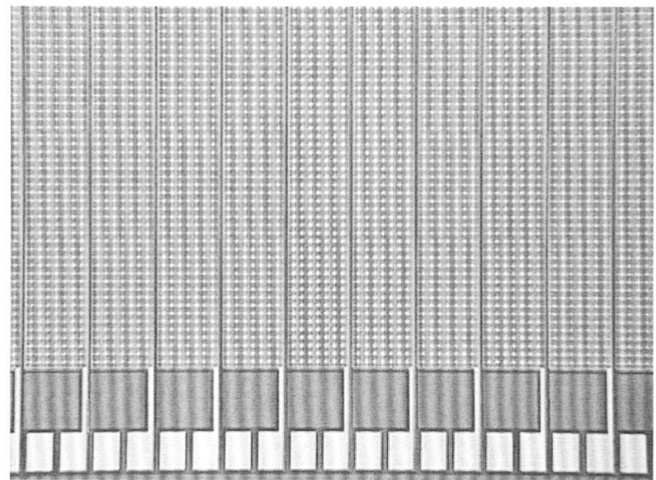

Fig. 3. A 128 element array of 36-μm × 36-μm CMUTs with a 0.34-μm-thick silicon membrane.

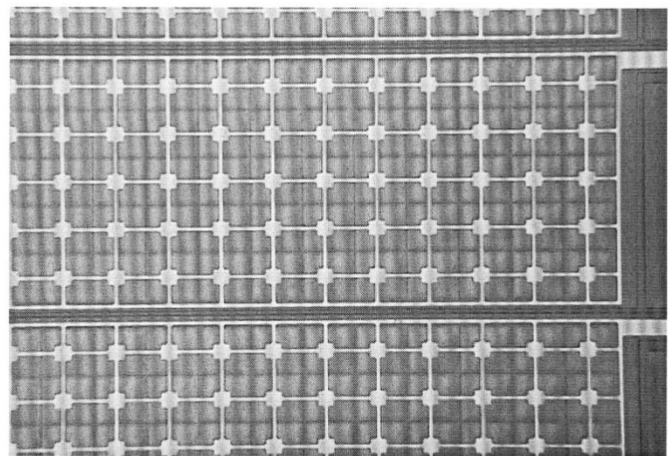

Fig. 4. Close view of a 128 element array of 36-μm × 36-μm CMUTs with a 0.34-μm-thick silicon membrane.

In the first fabrication run, an SOI wafer with an active layer thickness of 0.34 μm, which defined the membrane thickness, was used. The cell sizes of the membranes varied from 12 μm to 150 μm while the gap heights varied from 0.38 μm to 4 μm. The main reason for fabricating many designs was to explore what could be done with the new technique and what kinds of problems existed. Figs. 3–7 show images of fabricated devices. Table I summarizes the geometrical parameters of the designed devices. Hexagons and square shaped membranes were chosen to maximize the area efficiency of the devices.

In the second fabrication run, SOI wafers with an active layer thickness of 4.2 μm were used. The membrane size ranged from 600 μm to 750 μm (11.5 μm gap height). The electrode coverage was 100%. The fabricated devices were circular, 7.5 cm in diameter, and featured 10 100 membranes. They were divided into four quadrants each carrying a transducer with a different size membrane. The quadrants were independently wired and tested separately.

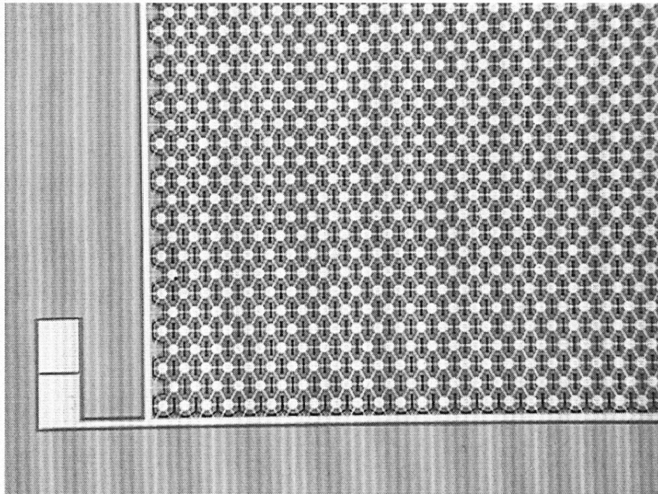

Fig. 5. A 7-mm × 7-mm CMUT array with 0.34-μm-thick silicon membrane.

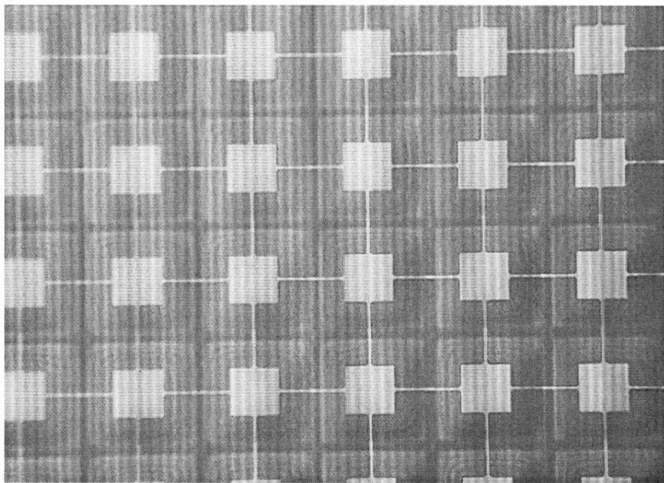

Fig. 6. A 10-mm × 10-mm array of 150-μm CMUTs with a 0.34-μm-thick silicon membrane.

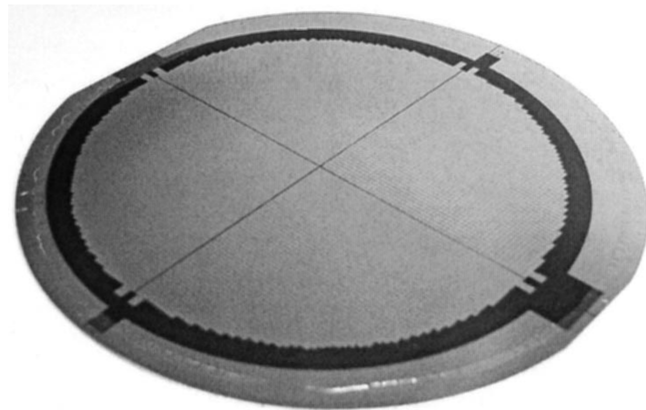

Fig. 7. A 75-mm diameter low-frequency CMUT array with 4.2-μm-thick silicon membrane. Four independent transducers are visible.

During this run, the peak deflection of the membranes was measured (5 repetitions) after each process step. By monitoring the deviation from the simulated values, it was possible to learn if stress had been introduced into the membranes during the preceding step. Predicted and measured values of atmospheric deflection, resonance frequency, bandwidth, collapse voltage, and ${k_T}^2$ are presented in Figs. 8–12, in the characterization part of the paper.

TABLE I
DESIGN PARAMETERS AND MEMBRANE DEFLECTION UNDER ATMOSPHERIC PRESSURE FOR VARIOUS SIZE SQUARE MEMBRANES

Membrane Size (μm)	Thickness (μm)	Ansys Result (μm)	Wyco Result (μm)
600	4.2	6.24	6.1
650	4.2	7.34	7.4
700	4.2	8.13	8.2
750	4.2	9.3	8.8
150	0.34	2.7	2.29-2.33
100	0.34	1.55	1.69-1.79
50	0.34	0.54	0.54-0.57
40	0.34	0.34	0.32-0.34
36	0.34	0.15	0.21-0.23
30	0.34	0.15	0.21-0.22
20	0.34	0.016	0.033-0.038
10	0.34	0.01	0.014

V. DEVICE CHARACTERIZATION

A. Mechanic Characterization

In order to fabricate CMUTs with desired operation characteristics, one needs to control the separation between the two electrodes of the device accurately [2]. Accurate determination of this separation requires precise control over the cavity depth and membrane deflection under ambient pressure. The cavity depth can be controlled precisely since it can be monitored during the cavity formation as described earlier. The other factor determining the electrode separation, the membrane deflection under ambient pressure, can with the wafer bonding technique be precisely controlled, too. The reason is that the two membrane parameters, internal stress and the material properties, which are difficult to control for LPCVD grown Si_xN_y in the traditional process, are now well controlled. In the silicon wafer bonding process, the membrane is made of single crystal silicon featuring low internal stress and well-defined material parameters: Young's modulus (Y), Poisson's ratio (σ) and density (ρ).

The membrane deflection profile under ambient pressure can be predicted by a finite element method (FEM) analysis and can be measured with an interferometer. Fig. 8 shows a sample 3-D profile of a 150 μm square, 0.34 μm thick silicon membrane measured by an interferometer featuring a spot size of 1 mm (Wyko Optical Profiler, Veeco Instruments Inc, US). Table I summarizes the peak deflection measurements on different sized membranes and compares them with the values predicted by the FEM simulations. The similarity of the FEM and interferometer results, 5.0%±4.6% with two outliers removed, is a measure that indicates the degree of predictability and control that we have over the fabrication process, respectively. Thus, it is evident that we can design and produce to meet the device specifications using the wafer bonding technique.

Although single crystal silicon possesses very low internal stress, a stress distribution is induced into the membranes when

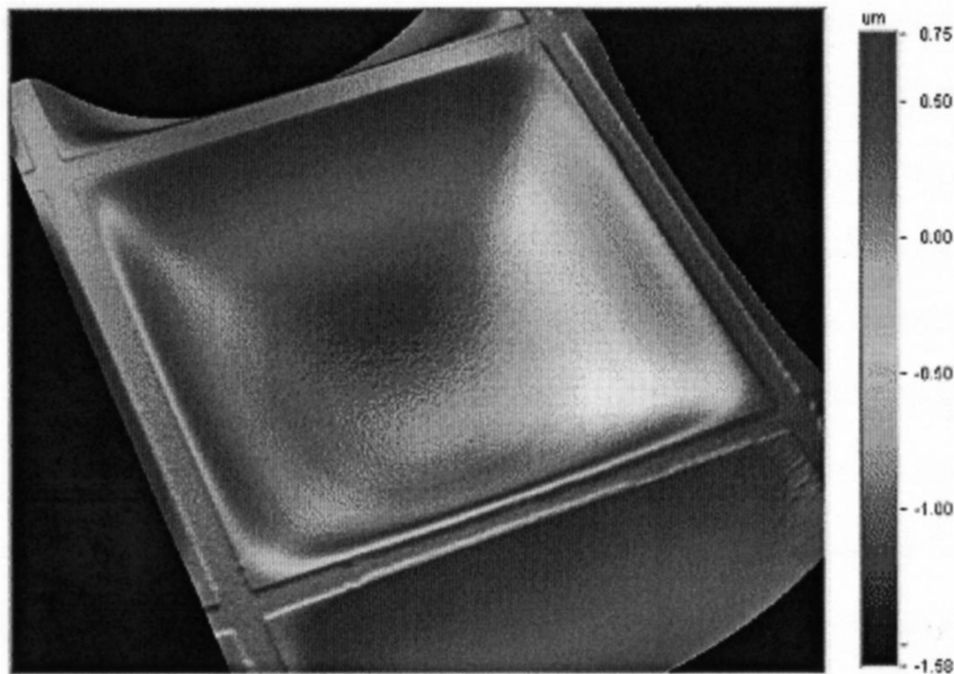

Fig. 8. Three-dimensional (3-D) profile of a 150-μm square, 0.34-μm-thick silicon membrane at atmospheric pressure measured with the interferometer. The supportive posts are clearly visible. The maximum deflection was 2.3 μm.

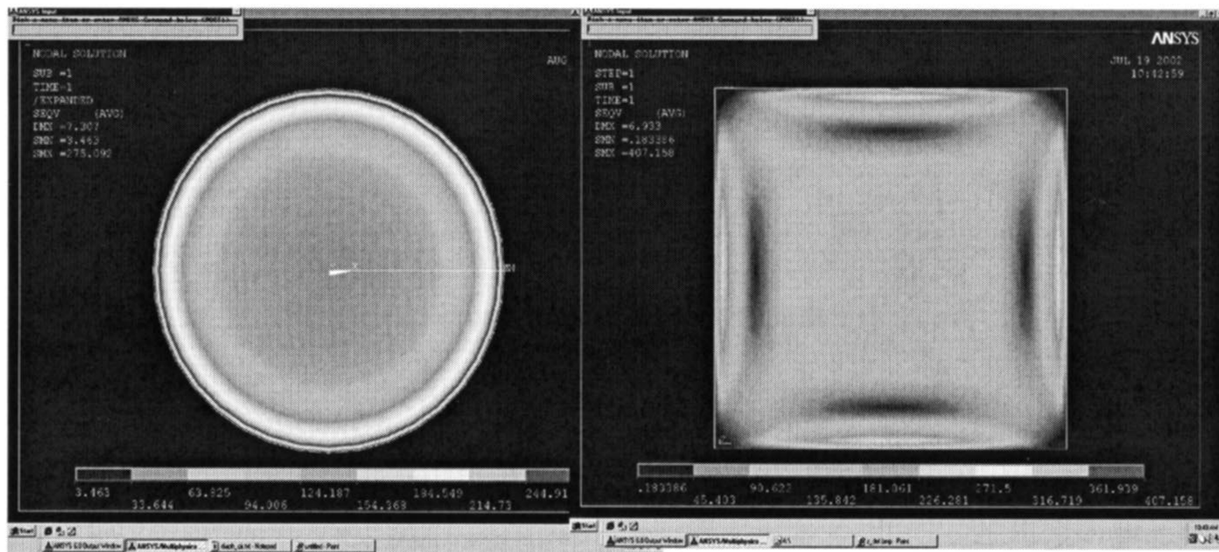

Fig. 9. Simulated stress distribution on a circular, 690 μm, and square membrane of comparative size, 650 μm.

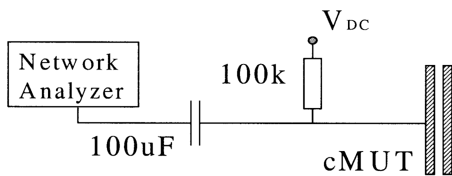

Fig. 10. Experimental setup to measure the electrical impedance of a CMUT.

they deflect under ambient pressure. The induced stress has an impact both on the dynamic behavior of the membrane and the process yield. FEM simulations take into account the induced stress distribution and predict the dynamic behavior of the membranes as described in the following subsection. The impact on the process yield is a result of the high local stress, that limits the size and thickness of a realizable membrane. For large or thin membranes, where large deflections occur, local stress may be high enough to create fractures in the membrane which easily propagate along a crystal axis.

The stress distribution within a membrane 650 μm by radius and 4.2 μm by thickness was simulated by Ansys, as described elsewhere [25] relying on the material parameters of ideal single crystal silicon, Y: 165 GPa, σ: 0.22 [26], and ρ: 2330 kg/m^3 [27]. The simulations were performed for circular and square shaped membranes to see the impact of the membrane shape on the local stress distribution. The simulation results, Fig. 9, show stress at a maximum of 400 MPa for the square membrane and 250

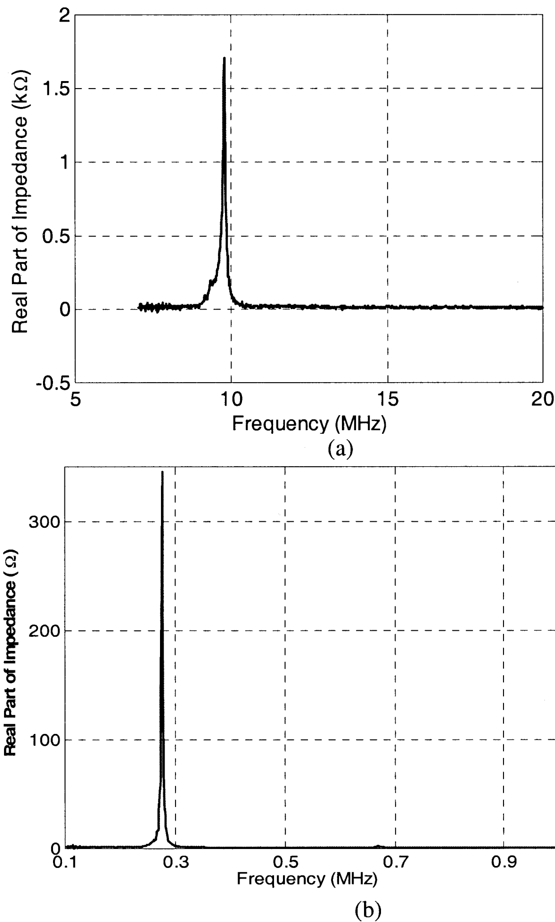

Fig. 11. The real part of the electric impedance of two CMUTs. One is designed for high-frequency operation (a) the other (b) is designed for low-frequency operation. The devices were analyzed when biased to 40 and 100 V, respectively.

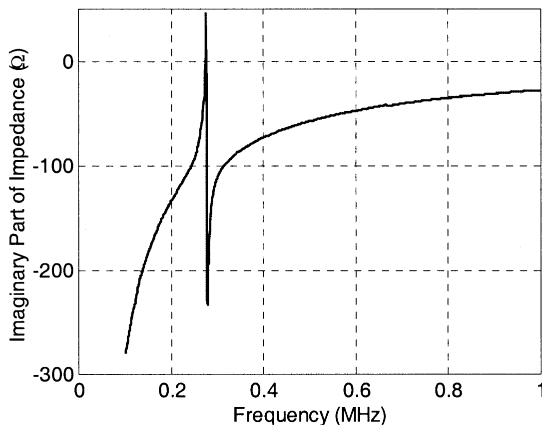

Fig. 12. The imginary part of the electrical impedance of a large CMUTdesigned for sub-MHz operation. The graph was obtained with the device biased to 100 V.

MPa for the circular membrane, and stress gradients in the membranes. (Since it is known that there is a $\pm 10\%$ thickness variation in the membranes, the distribution of which is unknown, the obtained simulation results can only be used as a guideline). These values are clearly well below the yield strength of single crystal silicon. Any defect in the crystal structure of the membrane will however, lower the yield strength into the hundreds of MPa range. Therefore, the yield of a fabrication run is partly determined by the number of defects in the membrane silicon, which is less than LPCVD grown low-stress Si_xN_y.

Another important process control step performed was to measure the membrane deflection after major process steps. The reason for this was to see if residual stress was induced into the membrane during the process steps in addition to that induced by deflection due to ambient pressure. The membrane deflection after each process step was measured with the interferometer, as mentioned previously, on the 650 μm diameter, 4.2 μm thick membranes. With each device the measurement was performed on five different membranes. The following measurements were carried out: 1) a deflection measurement before post anneal (7.38 ± 0.01 μm), 2) a deflection measurement after post anneal (7.28 ± 0.01 μm), and 3) a deflection measurement after aluminum deposition (7.15 ± 0.13 μm). The results show that there is no significant change in the membrane deflection as a result of the post-anneal. The decrease in the peak deflection after the Al deposition is a result of the tensile stress within the Al film. It is seen that silicon does not change during the annealing. The probability of identical average deflection p is 0.06 on a 0.05 confidence level. It is also seen that the deposition of aluminum doesn't significantly reduce the deflection ($p = 0.19$ on a 0.05 confidence level). Knowing the way in which the process steps modify the internal stress of the membrane makes it possible to predict the final position of an unbiased membrane.

Finally, it was concluded that we can predict, see the ANSYS results (7.3 μm versus 7.15 ± 0.13 μm), the membrane deflection with 5% accuracy. This is better than what was achieved with the traditional CMUT processing technique, 10% [28]. It is, moreover, seen that the new process produces the same deflection among devices in a specific run, 2%, as well as between devices in different runs, 5%. The measured membrane deflection results are similar between different finished wafers and different process runs. This indicates that the fabrication is well controlled.

In conclusion, the measured membrane deflection results are similar between different finished wafers and different process runs, indicating that the fabrication is well controlled. Furthermore, the measured membrane deflections matched those predicted by simulation indicating that the devices are well modeled and that the process is predictable. The detailed results are listed in Table I.

B. Electric Characterization

In order to assess how well controlled the fabrication process was, the fabricated devices were electrically characterized. The electrical characterization of a CMUT provides a first proxy of the acoustical activity of the transducer. This characterization was performed with a vector network analyzer (HP 8751A) that measured the complex input impedance of the transducer in air (the applied ac was -30 dBm corresponding to 10 mV across 50 Ω). The impedance was measured at several different bias voltages to get the impedance-bias voltage, $Z(V_{dc})$, curve. The measurement setup is shown in Fig. 10. The network analyzer was connected to the CMUT through a capacitor that blocked the dc bias, but allowed the ac signal to pass. The dc bias was

TABLE II
THE SIMULATED VERSUS MEASURED VALUES OF RESONANCE FREQUENCY, COLLAPSE VOLTAGE OF A 650-μm DIAMETER 4.2-μm-THICK CMUT MEMBRANE. THE MEASUREMENTS WERE PERFORMED IN AIR. THE BIAS VOLTAGE WAS 100 V

	Resonance frequency (kHz)	Membrane deflection (μm)	Collapse voltage (V)	k_T^2 (100V)
Ansys	310	7.3	132	0.35
Measured	306	7.28	130	0.25

supplied through a resistor that was small compared to the dc resistance of the CMUT to provide a constant dc voltage across the transducer.

The impedance measurements allowed the parameters of the electrical branch of the model circuit describing the transducer be analyzed [2]. Resonance frequency and bandwidth of the acoustically lightly loaded devices were first obtained. A peak in the real part of the impedance curve revealed vibratory motion in the device. This was an indication of acoustic activity. By comparing the center frequency of the measured resonance to the predicted resonance value it was possible to see that the simulated resonance frequency for the device was realized in the actual device. The height of the peak relative to the baseline and noise level gave an estimate of the acoustic efficiency of the device. The maximum real impedance divided by the device capacitance was used as a figure of merit for the device.

The imaginary part revealed two aspects of the device: the total device capacitance [2], [18] (active, C_0, and parasitic, C_p, capacitance) and the collapse voltage of the membrane. From the device capacitance curve it is possible to estimate the electro-mechanical coupling coefficient, $k_T{}^2$, of the device from the ratio of fixed capacitance to free capacitance. Here $k_T{}^2 = 1 - \mathrm{C_{fix}/C_{free}}$ where the fixed capacitance is the device capacitance at a given bias voltage and free capacitance is $\mathrm{d(VC_{fix})/dV}$ at the same bias voltage [18]. The parasitic capacitance obtained from the imaginary impedance curve is important since it determines the bias voltage required for a certain $k_T{}^2$ value [20]. From the capacitance curve, membrane collapse can be identified as an abrupt change in the device capacitance when increasing bias voltage. The reverse phenomenon, membrane snapback can also be detected from the capacitance curve when decreasing the bias voltage.

In the following, some of the electrical characterization results obtained are presented. These results prove the functionality of the fabricated devices and indicate the degree of predictability of the wafer bonding fabrication in terms of achieving the design parameters, e.g. center frequency, bandwidth and collapse voltage. The results also gave an indication of what can be fabricated at this state of process development. A more thorough characterization will be presented in a later paper.

Fig. 11 shows the measured real part of the impedance of two devices. One was designed for sub-MHz operation (membrane diameter 650 μm, membrane thickness 4.2 μm and gap height 4 μm), and one was designed for operation on a higher frequency (membrane diameter 20 μm, membrane thickness 0.34 μm and gap height 0.3 μm). The low frequency device is an efficient acoustic source ($\mathrm{Re\{Z_{max}\}/Re\{Z_{base}\}} = 400$) as is the high frequency device ($\mathrm{Re\{Z_{max}\}/Re\{Z_{base}\}} = 100$). The center frequency was 306 kHz and the bandwidth was 2 kHz, corresponding to an electrical Q of 145. This compares with the simulated center frequency value, 310 kHz. Fig. (11b) shows the corresponding plot measured on a device from another run. Here $\mathrm{f_o}$ is 9.8 MHz and BW is 0.1 MHz, corresponding to an electrical Q of 98.

The imaginary impedance of the low frequency device is shown in Fig. 12. A reactive load, approximately one fifth of the resistive load of the low frequency device at resonance, indicates that tuning out the capacitive reactance can be done with a small inductor. The significance of this is that a small inductor does not reduce the bandwidth as much as a larger inductor would. For this device the capacitance $(C_p + C_o)$ was 4.6 nF. This value compares with the simulated value that was 4.2 nF.

The predictability of the fabrication is seen in Table II, where design values versus measured values of resonance frequency and collapse voltage are tabulated for several low frequency devices.

VI. DISCUSSION

The prime outcome of the investigation is that it is possible to build working CMUTs with the wafer bonding technique. The experimental results indicate that the process is predictable, i.e., the devices perform according to the predicted simulation performance. This is not too surprising since wafer bonding is an established discipline. The wafer bonding technique appears, in light of the characterization results, to be able to produce, in a controlled manner, devices the operation of which are predictable, Table I and Table II. The uniformity, in terms of center frequency across the wafer, of the wafer bonding technique is also superior (0.3% versus 3%), to that achieved by the traditional technique. The reason lies probably in the wide specifications of the LPCVD process in terms of gas concentration, pressure and temperature.

Although the wafer bonding technique requires a high up-front investment in the form of expensive SOI wafers (approximately \$250 versus \$15 for 4-inch wafers) the shorter process run (1 week versus 4 weeks) and the need for fewer process steps (15 versus 22) should offset the initial cost. A shorter process run translates directly into faster turnaround while a reduction in the number of process steps translates into higher yield.

Another advantage of the new technique is that it makes it possible to fabricate large membranes that are needed for devices operating at low frequency (<200 kHz). Current wafer bonded CMUTs feature 750-μm-wide membranes compared to 180 μm wide membranes in traditionally fabricated CMUTs. The wafer bonding technique also increases the area efficiency

(active area per device face area) of devices fabricated for operation at high frequency (>20 MHz). This translates into higher transduction efficiency both in transmit and receive mode [20], as well as into lower secondary reflections from the transducer surface in pulse-echo operation.

Furthermore, the membrane and the cavity definitions can be made independent of each other, which can give advantages with unsealed air devices but probably not with vacuous devices where no resonator exists behind the membrane. Finally, with the wafer bonding technique complex structures can be fabricated with less effort than with the classic fabrication technique. Examples would be corrugated membranes for sensitivity, membranes loaded with a center mass to have more piston-like movement, and patterning of the cavity to decrease the parasitic capacitance of the device.

The largest membranes fabricated during this investigation were found to break easily along the cavity edges due to local high stress levels, as shown in Fig. 9. This was remedied by rotating, before bonding, the SOI wafer 10° to misalign the crystal axes of the SOI wafer with the cavity edges. Breaking of the membranes along the edges of the 1 to 2-μm-thick supporting posts is probably going to be an important question to tackle, especially if large membrane deflections are required.

The fabricated devices also showed a tendency to get charged (approximately in one day of operation). This degraded their transduction efficiency since the induced polarization reduced the effective bias across the capacitive transducer. The reason for the charging is not clear but it could be remedied by reversing the polarity of the bias voltage. Another problem encountered, which also is believed to be related to the charging, was electrical breakdown in the oxide or air gap at dc bias voltages above 100 V. The reason for this is not clear either. One possible explanation is that the unprotected Si surface attracts impurities (ions) that change the surface conductivity of any unprotected surface (This increased demand on purity might decrease the yield and drive costs in the form of higher demand on clean room level). This kind of surface charges result in parallel conductive paths that act as starting points for electric break down. It is believed that applying a thicker layer of oxide to protect any bare silicone surface could reduce the problem. This solution can, however, result in worse bonding especially if the flatness of the wafer is changed due to coverage of sharp steps.

Perhaps the most serious uncertainty of the new technique is that it relies on using a Si membrane. Compared to SiN, used with the classical technique, Si is not an insulator. This feature was aggravated by the fact that the devices fabricated utilized low-resistivity Si that made the membrane conductive and at the same time increased the parasitic capacitance. To reduce the parasitic capacitance, it would be possible to use high resistivity Si with a patterned metal electrode. This solution would share features with membranes fabricated with the traditional process. There would still remain the question of the metal-silicon stack whose electrical impact on the device operation is not yet known.

In addition to the aforementioned question about the high-resistivity Si membranes, effort should be committed to obtain the ultrasonic characteristics of the new devices. This would make it possible to quantitatively compare the new technique with the classical one when it comes to high-yield fabrication of transducers of various sizes with high dynamic range in a large frequency interval.

VII. Conclusion

This paper presents the first CMUTs fabricated with a wafer bonding technique. CMUTs with membranes of different size and thickness have been fabricated. The mechanical and electrical characterization performed on the devices indicated that they operated as was expected from the design. Compared to surface micro machining techniques, the wafer bonding technique shows a higher degree of predictability and involves fewer process steps that reduce the process turnaround time and potentially increases the yield. The new technique sets less process limitations on the size and shape of the membrane and the cavity. As a result it was possible, for the first time, to fabricate sub-MHz CMUTs.

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